REMARKS

To expedite prosecution, the applicant has amended claims 1, 6, and 10. Claim 18 has been cancelled. Claim 1 has been amended to incorporate the limitations of claim 18. Independent claims 6 and 10 have been amended to include limitations similar to those of claim 1.

Claims 1, 2, 4-6, 8-10, and 12-17 are pending in the application. The applicant respectfully requests reconsideration in view of the amendments to the claims and the following remarks.

I. The § 103 Rejections

Claims 1-2, 5 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,574,213 (Anandakumar).

Claims 4, 6, 8-10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anandakumar as applied to claim 1, and further in view of U.S. Patent No. 6,526,131 (Zimmerman).

Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Anandakumar in view of Zimmerman, and in further view of U.S. Patent No. 6,449,269 (Edholm).

The applicant respectfully traverses.

Claim 1 has been amended to include the limitations of claim 18 and recites a processor that includes one or more IEEE 802.3 media access controllers (MACs) and a repeater that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core.

A potential advantage of such a processor including a MAC and repeater integrated onto a same chip as the processor is that the processor can be directly connected to a local area network LAN, as shown in FIG. 1 (specification, col. 3, ll. 31-33).

A. Anandakumar Fails To Disclose An IEEE 802.3 Media Access Controller Integrated Onto A Same Chip As A Voice-over-IP Processor Core

As acknowledged by the Examiner, Anandakumar fails to disclose one or more MACs integrated onto a same chip as a processor. The Examiner, however, suggests that it would have been obvious to one of ordinary skill in the art to modify the DSP processor 1511 of Anandakumar such that the MCU controller 1781 and the DSP processor 1511 are integrated onto a same chip because "Anandakumar discloses various parts of functions of the DSP and Microcontroller can be partitioned and stored-on chip as desired (see col. 39, lines 1-10)." The applicant respectfully disagrees.

In the cited portion, Anandakumar discloses that adaptive rate/diversity operations (discussed in connection with FIG. 16) can be partitioned between various processors and the microcontroller of Anandakumar, and the adaptive rate/diversity operations can be stored in on-chip or off-chip memories. Anandakumar, however, does not suggest in the cited portion that functions associated with the processor and the microcontroller (apart from the adaptive rate/diversity operations) can be partitioned and stored onto a same chip.

B. Anandakumar Fails To Disclose A Repeater Integrated Onto A Same Chip As A Voice-over-IP Processor Core

As is commonly known in the art, a repeater is a network device that repeats signals from one cable onto one or more other cables. Anandakumar discloses a DSP processor 1511 including a echo canceller block 1517 and a gain control block 1521. In the Action, the Examiner associates a repeater with the combination of the echo canceller block 1517 and gain control block 1521. The applicant respectfully disagrees. While the echo canceller block 1517 may remove interference and the gain control block 1521 may strengthen signals (as acknowledged by the Examiner), the echo canceller block 1517 and the gain control block 1521 only does so in connection with signals received from the PCM interface 1515. The echo canceller block 1517 and the gain control block 1521 does not repeats signals from one cable onto one or more other cables, as would a repeater. Anandakumar, therefore, fails to disclose a repeater integrated onto a same chip as a voice over processor core, as required by claim 1.

C. The Claim Has Limitations Not Taught By Any Of The Cited References Above

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "**All** words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970) (emphasis added). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability. . . . If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Anandakumar fails to disclose a processor that includes one or more IEEE 802.3 media access controllers (MACs) and a repeater that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core. The Examiner has not shown that Zimmerman or Edholm discloses a processor that includes one or more IEEE 802.3 media access controllers (MACs) and a repeater that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core. Consequently, neither Anandakumar, Zimmerman, nor Edholm (either alone or in combination) can render claim 1 obvious, and the Examiner has not made a *prima facie* showing of obviousness.

D. No Motivation To Modify Anandakumar

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. The teaching or suggestion to make the claimed combination must be found in the prior art. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The applicant respectfully submits that the Examiner has not provided any teachings from Anandakumar that support modifying Anandakumar such that the MCU controller 1781 and the DSP processor 1511 are integrated onto a same chip.

1. The Examiner Has Shown No Objective Teaching

In making a rejection under § 103, the Examiner can satisfy the burden of making a *prima facie* case of obviousness "only by showing some objective teaching." *In re Fritch*, 972 F.2d 1260, 1265 (Fed. Cir. 1992). As has often been noted, evidence of teaching or suggestion is "essential" to avoid the error of hindsight. *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988).

"The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citation omitted).

The Examiner's proposed motivation for modifying Anandakumar is that it would have been obvious to modify Anandakumar to integrate the MCU controller 1781 and the DSP processor 1511 onto a same chip in order to consolidate both VoIP processing and physical network interfacing functions in the same chip so that data and signaling communication overhead time between the MCU controller 1781 and the DSP processor 1511 will be shorter. This does not constitute a showing of some objective teaching – either in the references or in any other source. The invention of Anandakumar is not directed to reducing data and signaling communication overhead between the MCU controller 1781 and the DSP processor 1511. Instead, it is a classic case of hindsight reconstruction.

Hindsight reconstruction, using applicant's claim as a template to reconstruct the invention by picking and choosing isolated disclosures from the prior art, is impermissible. For example, in *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), the Federal Circuit stated:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. (citations and quotations omitted)

The applicant respectfully submits that the Examiner has not provided any motivation to modify Anandakumar other than to rely on the level of skill in the art, which is impermissible. *See Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

E. Other Independent Claims

Claims 6 and 10 incorporate limitations similar to those of claim 1. Claims 6 and 10 (and the claims that depend therefrom) are also allowable over Anandakumar, Zimmerman, and Edholm for reasons corresponding to those set forth with respect to claim 1.

No fees are believed due, however, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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